

**Remarks/Arguments:**

**Claim Status**

Claims 41 and 42 are pending in the present Office Action.

By this response claims 41-42 are amended.

No new matter is presented by the claim amendments and, accordingly, entry and consideration are respectfully requested. Support for the claim amendments can be found throughout the original specification and, more particularly, for example, in the original specification at page 44, line 23 to page 45, line 5 and FIG. 6.

**Specification Objection**

In the Action at item 2, the specification is objected to for informalities therein related to claims 41 and 42.

Although it is believed by Applicants that amendments to the claims are not necessary because one skilled in the art would understand the meaning of claims 41 and 42 and would appreciate that the specification supports the language of these claims, Applicants have amended claims 41 and 42 to further clarify these claims and to improve the form of these claims such that the specification fully supports these claims. (See the specification at page 44, line 23 to page 45, line 5.)

Reconsideration is respectfully requested.

**Rejection of Claims 41 and 42 Under 35 U.S.C. §112, First Paragraph**

In the Action at item 3, claims 41 and 42 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement.

Reconsideration is respectfully requested.

The Examiner contends in the Office Action that the specification does not teach a signal having 2<sup>S</sup> internal states. Applicants respectfully disagree with the Examiner's contention but have made minor amendments to the claims to expedite prosecution. Claim 41, for example, now recites "a signal having a format related to a signal encoded by a convolutional encoder

having  $2^{(s+1)}$  internal states". This recitation is supported, for example, in the specification by FIG. 6, a combination of a comb filter and a 4-state decoder being used such that data passing through the comb filter may be considered as being an 8-state trellis-encoded signal. In particular, by using such a combination of the comb filter and the 4-state decoder, as depicted by FIG. 7, mapping points for the 4-state trellis encoder are 7, 5, 3, 1, -1, -3, -5 and -7 and when the comb filter is used on the receiving side, the outputs of the comb filter are 8-state signals at 15 levels (e.g., -14, -12, -10, -8, -6, -4, -2, 0, 2, 4, 6, 8, 10, 12, 14). This is because the comb filter performs arithmetic subtraction, as is depicted in FIG. 9B.

### **Rejection of Claims 41 and 42 Under 35 U.S.C. §112, Second Paragraph**

In the Action at item 4, claims 41 and 42 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

Reconsideration is respectfully requested.

The Examiner further contends in the Office Action that the recitation of "decoding the converted signal using the state transition having  $2^s$  internal states" does not make sense and thus, has interpreted  $2^s$  internal states in claims 41 and 42 to actually mean  $2^{s+1}$  internal states.

Applicants disagree with the Examiner regarding the interpretation given by the Examiner. Referring to the original specification, page 46, lines 11-20, at least one advantage of the exemplary embodiments of the present invention recited in claims 41 and 42 is that these trellis decoders can be commonly used for 4-state and for 8-state transitions. As one example, FIG. 9A shows an 8-state transition diagram. Further, the state transition diagram of FIG. 9A can be represented as that shown in FIG. 9D when represented internal states of D0 are considered as being ignored due to the use of the comb filter. Moreover, FIG. 9E illustrates relationships between branches in FIG. 9D and input X2X1 passing through each branch. In FIG. 9E, the lower bit X1 is obtained as normal Viterbi decoded data and the upper bit X2 is stored as a candidate for decoded data and is directly obtained after performing the Viterbi decoding. In this manner, it is possible to decode an 8-state received signal based on the four-state transitional diagram.

The Examiner also contends in the Office Action that the recitation of "a signal having  $2^{s+1}$  internal states" in claims 41 and 42 is unclear because the relationship between the "signal" and "internal states" of a state machine is omitted.

As above-mentioned, to expedite prosecution, Applicants have amended claims 41 and 42 from "converting ... into a signal having  $2^{s+1}$  internal states" to "converting ... into a signal having a format related to a signal encoded by a convolutional encoder having  $2^{s+1}$  internal states," to clarify the relationship between the signal and the internal states.

### **Rejection of Claims 41 and 42 Under 35 U.S.C. §102(b)**

In the Action at item 5, claims 41 and 42 are rejected under 35 U.S.C. §102(b) as being anticipated by Hu et al. (U.S. Patent No. 5838729) (hereafter referred to as Hu).

This ground for rejection is traversed.

The Office Action interprets " $2^s$ " in claims 41 and 42 to mean " $2^{s+1}$ ". Thus, the Examiner does not acknowledge that the distinguishing feature, as argued in response to the last Office Action, is present in the claim language.

### **Claim 41**

Claim 41 is directed to an error correction method, and recites "converting the received trellis-encoded signal into a signal having a format related to a signal encoded by a convolutional encoder having  $2^{(s+1)}$  internal states; and decoding the converted signal using the state transition diagram having  $2^s$  internal states". Claim 42 includes similar features. At least one advantage of the exemplary embodiments of the present invention recited in claims 41 and 42 is that such trellis decoders can be commonly used for 4-state and for 8-state transitions.

Figure 9A shows an 8-state transition diagram. The state transition diagram of FIG. 9A can be represented as that shown in FIG. 9D when represented internal states of D0 are considered as being ignored due to the use of the comb filter. FIG. 9E shows relationships between branches in FIG. 9D and input X2X1 passing through each branch. In FIG. 9E, the lower bit X1 is obtained as normal Viterbi decoded data and the upper bit X2 is stored as a candidate for decoded data and is directly obtained after performing the Viterbi decoding.

In this manner, it is possible to decode an 8-state received signal based on the four-state transitional diagram.

The inventions recited in claims 41 and 42 are capable of commonly decoding 4-state and 8-state encoded data based on a 4-state transition diagram. That is, these claimed inventions are characterized by decoding data having a large number of internal states (8-state) using data having a smaller number of internal states (4-state). That is, the inventions recited in claims 41 and 42 convert a received trellis-encoded signal having, for example, 4 internal states (i.e.,  $2^s$ , where  $s = 2$ ), into a signal having, for example, 8 internal states (i.e.,  $2^{(s+1)}$ , where  $s = 2$ ), and decode the converted signal using a state transition diagram having 4 internal states (i.e.,  $2^s$ , where  $s = 2$ ).

### **Hu Reference**

Hu discloses that regardless of whether a 4-state or a 8-state trellis-encoded signal is received, the received signal is decoded using an 8-state transition diagram. This is contrary to the present invention recited in claims 41 and 42 because the transition diagram used in Hu is not a 4-state transition diagram (i.e., the smaller of the above-mentioned 4 and 8 internal states). Hu discloses that "in the filtered mode when rejection filter 22 is used, an eight state trellis decoder is required, and in the non-filtered mode when filter 22 is not used, a four state trellis decoder is required, as known. Trellis decoder system 24 (Fig. 1) advantageously incorporates a single eight state trellis architecture and seamlessly switches between modes," (emphasis added; see column 5, lines 16-21). Moreover, Hu further discloses that the "inventors have recognized that an eight state ACS unit may be used to mimic the four state ACS architecture required for the non-filtered mode. This is because BMC unit 30 performs parallel equivalent computations to provide replicated branch metric values to ACS unit 43 in the non-filtered mode. The disclosed ACS structure not only emulates the desired four state ACS architecture when it is provided with the input replicated values, but also enables ACS unit 43 to operate the same way in filtered and non-filtered modes," (emphasis added; see column 5, lines 38-47). Thus, contrary to the present invention of claims 41 and 42 Hu discloses use of only a 8-state transition diagram when the number of internal states of the received signal is 4 or 8 states.

For at least the above-mentioned reasons, claims 41 and 42 patentably distinguish over Hu, and it is submitted that this rejection should be withdrawn.

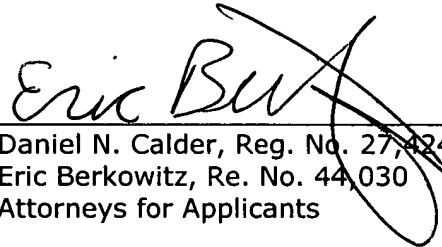
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**Conclusion**

In view of the claim amendments and remarks set forth above, Applicants respectfully submit that claims 41 and 42 are in condition for allowance and early notification to that effect is earnestly solicited.

Respectfully submitted,

  
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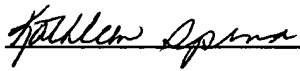
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